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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,391	03/31/2004	Jac-Bon Koo	61610120US	7644

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EXAMINER	
ZUBAJLO, JENNIFER L	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
09/28/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/813,391	KOO ET AL.	
	Examiner	Art Unit	
	Jennifer Zubajlo	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3-8 are rejected under 35 U.S.C. 102(b) as being unpatentable over Tsutomu Yamada (Patent No.: US 6,366,025).

As to claim 1, Yamada teaches:

A flat panel display, comprising: a plurality of pixels, where each of the plurality of pixels includes R, G and B unit pixels to embody red (R), green (G) and blue (B) colors (see figure 3 and 5 element 160 (R,G, and B) and column 6 lines 53-54), respectively, and where each of the unit pixels includes a transistor with multi gates, wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region (see figure 4) with a different geometric structure (figure 4, Abstract, and column 3 lines 16-23) between the multi gates from one another (see figure 4, column 6 lines 55-67, and column 7 lines 1-19).

Yamada fails to directly teach the unit pixels with R, G, and B subpixels. However, Yamada teaches R, G, and B as their own pixels, which each have their own transistors wherein transistors at least 2 pixels R, G, or B include a offset region with a

different geometric structure between the multi gates from one another (see figure 4). The transistors are not taught directly but it is inherent for a pixel to have a transistor. It would be obvious for each pixel R, G, and B to contain subpixels of R,G, and B to form unit pixels as described in claim 1 (see column 2 lines 56-57 "emissive regions 1B, 1R, and 1G for the display pixel").

As to claim 3 (dependent on claim 1), Yamada teaches the limitations of claim 1 for the reasons above. Yamada teaches total lengths of the offset regions between the multi gates of the transistors of the R, G, and B unit pixels are the same (see Figure 3), and offset lengths of a portion in the offset regions, where the portion is not doped with impurities, are different from one another (see Figure 4 and column 7 lines 3-19).

As to claim 4 (dependent on claim 3), Yamada teaches the limitations of claims 1 and 3 for the reasons above. Yamada teaches the R, G, and B unit pixels to each include a light-emitting device driven by the transistor (see column 2 lines 7-8, 30-32, 53-54, column 12 lines 16-18), respectively, where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light-emitting devices having a relatively lower luminous efficiency (see column 3 lines 28-44).

As to claim 5 (dependent on claim 1), Yamada teaches the limitations of claim 1 for the reasons above. Yamada teaches total lengths of the offset regions between the multi gates of the transistors of the R, G, and B unit pixels are the same (see Figure 3), and the offset regions have different widths from one another (see Figure 4).

As to claim 6 (dependent on claim 5), Yamada teaches the limitations of claims 1 and 5 for the reasons above. Yamada teaches the R, G, and B unit pixels to each include a light-emitting device driven by the transistor (see column 2 lines 7-8, 30-32, 53-54, column 12 lines 16-18), where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light emitting devices having relatively lower luminous efficiency (see column 3 lines 28-44).

As to claim 7 (dependent on claim 1), Yamada teaches the limitations of claim 1 for the reasons above. Yamada teaches the widths of the offset regions between the multi gates of the transistors of the R, G, and B unit pixels are the same (see Figure 3), and lengths of the offset regions are different from one another (see Figure 4).

As to claim 8 (dependent on claim 7), Yamada teaches the limitations of claim 1 for the reasons above. Yamada teaches the R, G, and B unit pixels to each include a light-emitting device driven by the transistor (see column 2 lines 7-8, 30-32, 53-54,

column 12 lines 16-18), where an offset length of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors is longer than an offset length of an offset region of transistors for driving light-emitting devices having relatively lower luminous efficiency (see column 3 lines 28-44).

3. Claims 2, 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutomu Yamada (Patent No.: US 6,366,025) in view of Mutsumi Kimura (Patent No.: US 6,529,213 B1)

As to claim 2 (dependent on claim 1), Yamada teaches the limitations of claim 1 for the reasons above. Yamada also teaches the R, G, and B unit pixels where each include a light-emitting device driven by the transistor (see column 2 lines 7-8, 30-32, 53-54, column 12 lines 16-18), where a resistance value of an offset region of a transistor for driving a light-emitting device having the highest luminous efficiency among the transistors of the R, G, and B unit pixels is higher than a resistance value of offset regions of transistors for driving light-emitting devices having a relatively lower luminous efficiency (see column 3 lines 28-44).

Yamada doesn't specifically refer to resistance values.

Kimura teaches a light-emitting device (18-1 and 18-2) driven by the transistors (16-1, 16-2, 17-1, 17-2) where the transistors have different resistance values (see column 2 lines 9-40, column 5 lines 24-29, and figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada with the different resistance values taught by Kimura to maintain an even light emission intensity.

As to claim 9, Yamada teaches a flat panel display, comprising: a plurality of pixels, where each of the plurality of pixels including R, G and B unit pixels to embody red (R), green (G) and blue (B) colors (see figure 3 and 5 element 160 (R,G, and B) and column 6 lines 53-54),respectively, and where each of the unit pixels includes a transistor with multi gates, wherein transistors of at least two unit pixels among the R, G, and B unit pixels each include an offset region (see figure 4, column 6 lines 55-67, and column 7 lines 1-19).

Yamada fails to directly teach the unit pixels with R, G, and B subpixels. However, Yamada teaches R, G, and B as their own pixels, which each have their own transistors wherein transistors at least 2 pixels R, G, or B include a offset region with a different geometric structure between the multi gates from one another (see figure 4). The transistors are not taught directly but it is inherent for a pixel to have a transistor. It would be obvious for each pixel R, G, and B to contain subpixels of R,G, and B to form unit pixels as described in claim 1 (see column 2 lines 56-57 "emissive regions 1B, 1R, and 1G for the display pixel").

Yamada doesn't teach an offset region having a different resistance value between the multi gates from one another.

Kimura teaches an offset region having a different resistance value between the multi gates from one another (see column 2 lines 9-40, column 5 lines 24-29, and figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada with the different resistance values taught by Kimura to maintain an even light emission intensity.

As to claim 10 (dependent on claim 9), Yamada teaches the limitations of claim 9 for the reasons above.

Yamada doesn't teach the unit pixels having different resistance values from one another each include light-emitting device, respectively, and the transistors for controlling currents supplied to the light-emitting device of each unit pixel.

Kimura teaches the unit pixels having different resistance values from one another each include light-emitting device, respectively, and the transistors for controlling currents supplied to the light-emitting device of each unit pixel (see column 2 lines 9-40, column 5 lines 24-29, and figure 6).

None of the references directly teach having channel layers with the same size however it would have been obvious matter of design choice since applicant has not disclosed channel layers of the same size solving any stated problem and it appears that channel layers of different sizes would perform equally well.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada with the different resistance

values and the transistors for controlling currents taught by Kimura to maintain an even light emission intensity.

As to claim 11 (dependent on claim 9) and 12 (dependent on claim 11), Yamada teaches the limitations of claim 9 for the reasons above. Yamada also teaches the R, G, and B unit pixels each include a light-emitting device driven by the transistor (see column 2 lines 7-8, 30-32, 53-54, column 12 lines 16-18), respectively, and resistance values of offset regions of the transistors are determined by luminous efficiencies of the light-emitting devices driven by the transistors where the resistance value having the highest luminous efficiency among the transistors of the R, G, and B unit pixels is higher than a resistance value having a relatively low luminous efficiency (see column 3 lines 28-44).

Yamada doesn't specifically refer to resistance values.
Kimura teaches a light-emitting device (18-1 and 18-2) driven by the transistors (16-1, 16-2, 17-1, 17-2) where the transistors have different resistance values that are determined by luminous efficiencies of the light-emitting devices driven by the transistors where the resistance value having the highest luminous efficiency among the transistors of the R, G, and B unit pixels is higher than a resistance value having a relatively low luminous efficiency (see column 2 lines 9-40, column 5 lines 24-29, and figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada with the different resistance values taught by Kimura to maintain an even light emission intensity.

4. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutomu Yamada (Patent No.: US 6,366,025) in view of Mutsumi Kimura (Patent No.: US 6,529,213 B1), further in view of Seung-Ki Joo (US 6,278,130 B1).

As to claims 13 and 15 (both dependent on claim 9), and 14 and 16 (dependent on claims 13 and 15 respectively), Yamada and Kimura teach the limitations of claim 9 for the reasons above.

Yamada and Kimura do not teach the offset regions of the transistors (at least 2 transistors) of the R, G, and B unit pixels doped with impurities having different doping concentrations from one another.

Joo teaches the offset regions of the transistors (at least 2 transistors) of the R, G, and B unit pixels doped with impurities having different doping concentrations from one another with different concentrations dependent on luminous efficiencies (see column 3 lines 36-50, column 4 lines 63-67, column 5 lines 57-65, and column 6 lines 32-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada and Kimura with the different doping concentrations of the offset regions of the transistors taught by Joo in order to alter the electrical properties to the desired effect.

Response to Arguments

5. Applicant's arguments (remarks), see pages 6-9, filed 8/7/2007, with respect to the rejection(s) of claim(s) 1 and 3-8 under 102(b) have been fully considered and are persuasive and also with respect to the rejection(s) of claim(s) 2 and 9-12. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yamada under 103(a) (see above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Zubajlo whose telephone number is (571) 270-1551. The examiner can normally be reached on Monday-Friday, 8 am - 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JZ
9/20/07

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER